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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,636	07/25/2003	Sang-Hyun Park	053933-5052	9623

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EXAMINER	
TRAN, NHAN T	
ART UNIT	**PAPER NUMBER**
2622	
MAIL DATE	**DELIVERY MODE**
07/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/626,636	PARK ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/25/2003 & 6/22/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-14* is/are allowed.

6)☒ Claim(s) *1-3,6,8 and 9* is/are rejected.

7)☒ Claim(s) *4,5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 7/25/2003 and 6/22/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objections

3. Claim 1 is objected to because of the recitation of *"a present data area storing second image data"* in lines 8-9 of claim 1. This should be corrected to read as -- *a present data area storing second* ***line*** *image data* -- to provide consistent claim terminology throughout claim 1 and all other dependent claims.

4. Claims 5, 7 & 10 are objected to because of the recitation of *"the same clock"* in the last limitation of each of claims 5, 7 & 10. This should be corrected to read as -- ***a*** *same clock* --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 6, 8 & 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki (US 7,116,358).

Regarding claim 1, Sasaki discloses a memory providing apparatus for an image data interpolation in an image processing system (see Figs. 1-3 and col. 16, lines 53-61) having an image sensor (CCD 21) outputting line image data from a sensed image (see col. 15, lines 30-39 and Fig. 14 for line buffer), comprising:

a readable and writable single memory (memory 29 shown in Fig. 2);

a buffer register (Fig. 14, buffer 62 comprising line buffers 21a, 61b; see col. 24, lines 33-38) having a prior data area (note that "a prior data area" is broadly recited and reads on buffer 61b) storing first line image data (Fig. 14), which has been stored in the memory (CCD image data buffer in memory 29 is read out to the buffer register of RPU 23 as disclosed in col. 16, lines 53-66), in a unit of 2m bits (2 x 8 bits as each pixel has 8 bits and the buffer is capable of storing 2 pixel data as one line when the camera is set to color mode shown in Fig. 10, col. 23, line 65), and having a present data area (buffer 61a) storing second image data (i.e., a second line of 2 pixels, each having 8

bits), which is inputted in a unit of m bits (8 bits), in a unit of the 2m bits (2 x 8 bits); and a memory controller (DMA 32) providing the memory with a chip enable signal, a write enable signal, and an address indicating locations of the first and second line image data stored in the buffer register (see Figs. 1, 2, 5 & 14 and col. 16, lines 53-66, wherein the chip enable signal, write enable signal and address indicating locations of the first and second line image data are inherent in the imaging system of Sasaki in order for the DMA to address, read and write the line image data into and out of the buffer and memory), reading and writing the first and second line image data from and on the memory (29), and outputting the first and second line image data and a third line image data (outputting to buffer register shown in Fig. 14 for processing and then storing in buffer 29b as processed data shown in Figs. 5, 14 & 17), which is inputted from the image sensor (CCD 21, it is noted that the input image data from CCD 21 can be direct or indirect which the claim does not require).

Regarding claim 2, Sasaki also discloses an image signal processor (RPU 23) performing an image interpolation (by block 42) when receiving the first, second, and third line image data from the memory controller (see Figs. 3 & 14; col. 16, lines 53-66 and col. 24, lines 33-45).

Regarding claim 3, Sasaki further discloses that the memory (29) is capable of storing a whole image frame having a plurality of 2 x 2 pixels shown in Fig. 10 which is stored in a memory cell of 4 x 8 bits (4m bits) data in an upper area (i.e., containing R

and G pixels in 2 x 8 bits data) and lower area (i.e., containing G and B pixels in 2 x 8 bits data). It is also clear that all bits data are readable and writable by the memory controller (Figs. 2, 3, 5, 10 & 14; col. 16, lines 53-66 and col. 23, line 65).

Regarding claim 6, Sasaki discloses that the memory controller comprises: three data transmission lines through which the first, second, and third line image data are outputted from the memory controller (see Figs. 5 & 14).

Regarding claim 8, it is clear in Sasaki that the line image data comprises a Bayer pattern (see Fig. 10 and col. 22, lines 23-25).

Regarding claim 9, Sasaki also discloses that the image sensor comprises a charge coupled device (CCD 21) image sensor.

Allowable Subject Matter

6. Claims 4, 5 & 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 10-14 are allowed.

(note that correction requirement for claims 5, 7 & 10 as set in section 4 should be complied before allowance)

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4, the prior art of record fails to teach or fairly suggest the limitations of claim 4, in combination with claims 3 & 1, including **"...the memory controller controls the chip enable signal and the write enable signal to be enabled and disabled, respectively, and reads the first line image data from the memory when the chip enable signal and the write enable signal are enabled and disabled, respectively, to store the first line image data in the prior data area of the buffer register, and the memory controller controls the chip enable signal and the write enable signal to be enabled, and stores the first and second line image data, which have been stored in the buffer register, in the memory in a unit of the memory cell unit."**

Regarding claims 5 & 7, the prior art of record also fails to teach or fairly suggest the limitations of each of claims 5 & 7, in combination with claims 3 & 1, including **"...first, second, and third data transmission lines through which the first, second, and third line image data are outputted from the memory controller, respectively, wherein the memory controller reads the first and second line image data stored in the memory, transmits the first and second line image data through the first and second data transmission lines, and transmits the third line image data, which is inputted from the image sensor, through the third data transmission line according to [the] same clock."**

Regarding claim 10, the prior art of record also fails to teach or fairly suggest the combination of all limitations required in claim 10 that includes **"...storing the first line image data of the present data area of the buffer register in a memory in the unit of the 2m bits; refreshing the buffer register; reading the first line image data from the memory in the unit of the 2m bits to store the read first line image data in a prior data area of the buffer register, and storing second line image data outputted from the image sensor in the unit of the m bits in the present data area of the buffer register in the unit of the 2m bits; storing the first line image data and the second line image data stored in the prior data area and the present data area of the buffer register, respectively, in the memory in a unit of 4m bits; and transmitting the first and second line image data stored in the memory and third line image data outputted from the image sensor to an image signal processor according to [the] same clock signal."**

Regarding claims 11-14, these claims are dependent from claim 10.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner